Digital Group Demodulation System for Multiple PSK Carriers

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In the near future, the onboard regenerative repeating system will be employed to convert many low-speed single channel per carrier (SCPC) signals to a high-speed time division multiplex (TDM) signal. Similar situations can be considered in a star network, where many small Earth stations communicate with terrestrial telephone stations through a large-size central Earth station. In both cases, many SCPC signals are concentrated and demodulated by a central station. Therefore, hardware and power consumption minimization is necessary. This demand resulted in a group modulator/demodulator concept. A group demodulator employs the same hardware effectively in common in demodulating multiple phase shift keying/frequency division multiplex (PSK/FDM) carriers. Actually, a transmultiplexer (TMUX) is used as a combination of a filter bank and down converters. Although a TMUX usually markedly reduces hardware, it introduces a new problem in demodulating an individual channel signal from the TMUX output. This problem is caused by a difference between a TMUX operation rate and each SCPC symbol rate. In this paper, an adaptive rate conversion filter is proposed to resolve this problem. In addition, each channel clock timing difference and carrier frequency offset are compensated for by channel demodulators attached individually to each TMUX channel output. The channel demodulator has been actually developed for 64 kb/s quadrature phase-shift keying (QPSK) signal and its performance has been evaluated. Using this technique, a 16 channel group demodulator has been manufactured.

Nomenclature

A = sampling data sequence
f_b = baud rate frequency, $= 1/T_b$
f_s = sampling frequency at the end of transmultiplexer, $= 1/T_s$
G = interpolation function
k = input sampling data number to filter
N = filter tap number
N_c = multiplexed carrier number
r = sign of a clock timing error
S = filtered output sequence
T_b = baud rate interval
T_c = timing control stepsize
T_d = sampling interval at the front of transmultiplexer
T_s = sampling interval at the end of transmultiplexer
α = phase offset
β = delay parameter in the filter
γ = phase increment caused by clock frequency difference between transmitter and receiver
τ = analog time variable

Introduction

IN a digital satellite communications system involving many small-capacity Earth stations, the SCPC/PSK method (single channel per carrier with phase shift keying) is usually adopted as the pertinent multiple-access technique providing an economical system. The reason is that HPA power and antenna size for each SCPC station can be reduced, compared with the time division multiplex access (TDMA) system for the same transmitting capacity. It also provides an easy entry system for personal users.

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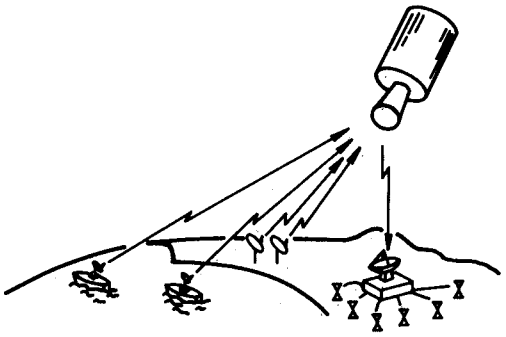
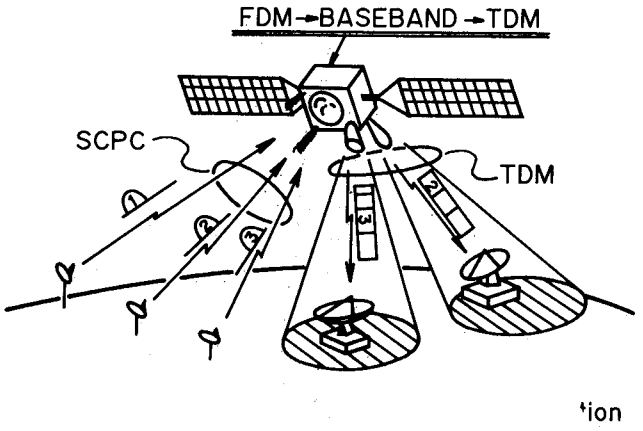
A coastal Earth station involved in maritime satellite communications,[1] such as shown in Fig. 1a, and a head office Earth station gathering information from branch offices through a business satellite communications system (which modulates and demodulates many PSK carriers in a station) are typical SCPC examples of star networks. For terrestrial communications, another typical example is a base station in a point-to-multipoint network system using this method. A problem anticipated with such stations is that the required hardware size may grow linearly as the number of channels increases. Assuming that conventional demodulators are used, each of which consists of channel-basis elements, a bandpass filter, a down converter, a clock timing recovery circuit, a carrier recovery circuit, etc., the system rapidly becomes very large. Therefore, a method of using, as much as possible, common hardware in place of channel-basis elements is required. Since SCPC/PSK signals are arranged with regular carrier spacing, individual bandpass filter and down converter elements can be replaced with the well-known transmultiplexer technique,[2,3] forming a filter bank. This efficient arithmetic algorithm, based on digital signal processing, drastically reduces the size of the hardware. If the system size can be adequately reduced, onboard regenerative communications[4] such as shown in Fig. 1b can be realized. In this paper, actual approaches are discussed to realize a compact-sized demodulator called a "group demodulator" capable of demodulating multiple SCPC signals simultaneously.

Digital Group Demodulator

Figure 2 shows the digital group demodulator configuration. Intermediate-frequency (IF) PSK multiple carrier signals are converted to a complex baseband signal in a block by a frequency converter. Then, its real and imaginary components are individually sampled at the rate of N_c times the carrier spacing for demodulating N_c PSK carriers in common by two analog/digital (A/D) converters. Individual output/input spectra are also shown in Fig. 2. By use of Transmultiplexer (TMUX) as a filter bank in place of many bandpass filters and down converters, the sampled multiplexed PSK carrier signal is simultaneously converted into complex baseband PSK signals. In a multicarrier SCPC/PSK system, each Earth station transmits PSK signals having individual carrier frequen-



a) Message service using SCPC.



b) Onboard regenerative communications.

Fig. 1 Various future services.

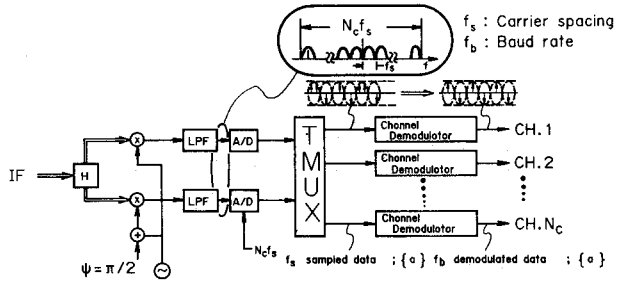


Fig. 2 Digital group demodulator configuration.

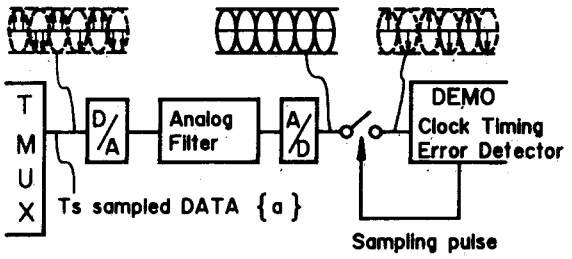
thermore, the received signal level differs from carrier to carrier. Consequently, a channel demodulator having a carrier recovery, clock recovery, and automatic gain control (AGC) function is arranged for each TMUX channel output, as shown in Fig. 2.

The group demodulator employing the TMUX requires two A/D converters to change a group signal of N_c SCPC carriers to N_c individual digital signals at a T_d sampling interval. T_d and the TMUX operation interval T_s are usually selected as

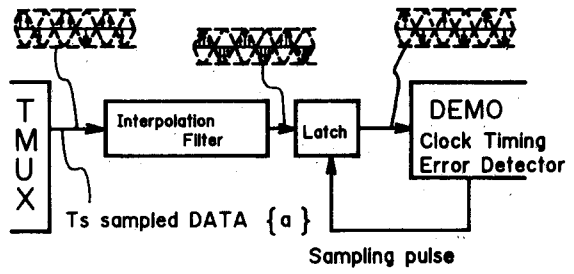
$$T_d = (1/N_c)(1/f_s)$$
$$T_s = 1/f_s \tag{1}$$

where f_s is the SCPC carrier spacing frequency.

In general, the f_s value is chosen to be 1.4-1.6 times the



a) Analog filter interpolation.



b) Digitak filter interpolation.

Fig. 3 Interpolation methods.

symbol rate f_b, from the view point of frequency utilization efficiency. Thus, the TMUX does not produce baud rate output, from which the transmit data should be decided. Consequently, a time-variant (adaptive) interpolation function is required for generating the T_b sample sequence signal from the T_s sample sequence in a time-variant manner.

Channel Demodulator

As stated previously, the channel demodulator must include an interpolation circuit, a clock timing recovery circuit, a carrier recovery circuit, and an AGC circuit. In this section, an adaptive rate conversion (ARC) filter is proposed and the overall design for the channel demodulator is disclosed.

Rate Conversion Filter

An analog interpolation approach, shown in Fig. 3a, requires extra A/D and D/A converters for each channel. An equivalent digital approach, shown in Fig. 3b, requires too much computation to be efficiently realized. Therefore, neither of these approaches can be considered to be optimum from a hardware complexity viewpoint. A remaining approach is the use of a rate conversion filter algorithm, perhaps including some sort of adaptation.

The basic rate conversion (RC) filter algorithm is explained as follows.

Consider an interpolation filter with an impulse response $G(t)$ that takes in the output data sequence $\{A(nT_s)\}$ from the TMUX. The output signal is given as

$$S(\tau) = \sum_{n=-\infty}^{\infty} A(nT_s)G(\tau - nT_s) \tag{2}$$

If the output signal is sampled every $T_b (= 1/f_b)$ interval, Eq. (2) is modified to give an output sample as

$$S(mT_b) = \sum_{n=-\infty}^{\infty} A(nT_s)G(mT_b - nT_s) \quad (m,n = 1,2,3,\ldots) \tag{3}$$

Figure 4 shows a time domain relation between sampled values $\{A_j\}$ and interpolated baud rate values of the $\{S_m\}$. $\{S_m\}$ and $\{A_j\}$ sequences in Fig. 4 correspond to the $S(mT_b)$ and $A(jT_s)$ sequences, respectively. The time difference $\beta^{(m)}$ between mT_b and the sampled time just prior to A_j is defined as

$$\beta^{(m)} = mT_b - jT_s \tag{4}$$

Then, Eq. (3) can be expressed as

$$S(mT_b) = \sum_{n=-\infty}^{\infty} A(nT_s)G(jT_s + \beta^{(m)} - nT_s) \tag{5}$$

Using a new variable i introduced as $i=j-n$, Eq. (5) is modified as

$$S(mT_b) = \sum_{i=-\infty}^{\infty} A\{(j-i)T_s\}G(iT_s + \beta^{(m)}) \tag{6}$$

As $k^{(m)}$ is a number of sampled data between S_{m-1} and S_m in Fig. 4, j in Eq. (6) is expressed as

$$j = \sum_{L=0}^{m} k^{(L)} \tag{7}$$

Therefore, Eq. (6) is modified as

$$S(mT_b) = \sum_{i=-\infty}^{\infty} A\left\{\left(\sum_{L=0}^{m} k^{(L)} - i\right)T_s\right\}G(iT_s + \beta^{(m)}) \tag{8}$$

where N is a number of transversal filter taps.

When $|i|$ becomes large, $G(iT_s)$ approaches zero. So, $S(mT_b)$ can be well approximated by using only partial terms in the $-N/2 \sim i \sim N/2$ range. Therefore, the rate conversion filter is expressed as

$$S(mT_b) = \sum_{i=-N/2}^{N/2} A\left\{\left(\sum_{L=0}^{m} k^{(L)} - i\right)T_s\right\}G(iT_s + \beta^{(m)}) \tag{9}$$

Equation (9) is the rate conversion filter algorithm for converting from T_s interval data to T_b interval data.

In an actual case, one concept for looking for $k^{(m)}$ and $\beta^{(m)}$ values is expressed as

$$k^{(m)} = \text{int}\left[\frac{T_b + \beta^{(m-1)}}{T_s}\right]$$

$$\beta^{(m)} = T_b + \beta^{(m-1)} - k^{(m)}T_s \tag{10}$$

where int $[x]$ implies maximum integer not to exceed the value of x. These equations are easily understood from Fig. 4.

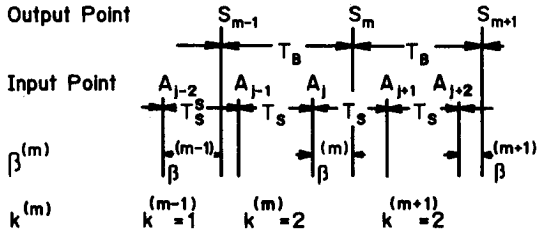


Fig. 4 $\{S\}$, $\{A\}$, and $\beta^{(m)}$, $k^{(m)}$ relation.

Adaptation Algorithm for Rate Conversion Filter

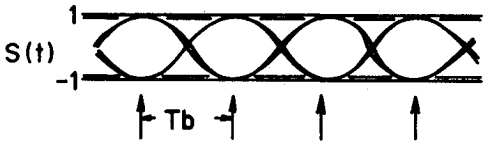
Theoretically, eye-opening data for interval T_b can be obtained from TMUX output data for interval T_s by the rate conversion filter. Actually, a clock phase offset and clock frequency difference exist between the transmitter and receiver sides, so the eye-opening data cannot be obtained without any time-variant adaptation. Therefore, the rate conversion filter must be so controlled that the sequence $\{S(mT_b)\}$ continues to be the optimum eye-opening value. This adaptation is basically performed by compensating for inaccurate transmit timing.

This incorrect timing is detected by a double-simpling method.[5] When $\{S(mT_b)\}$ defines the value of an eye-opening point (see Fig. 5a), the interpolated value $T_b/2$ separate from the eye-opening point, $\{S[(m-\frac{1}{2})T_b]\}$, is generated as

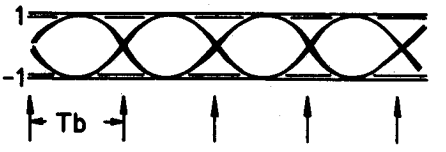
$$S\{(m-\tfrac{1}{2})T_b\} = \sum_{i=-N/2}^{N/2} A\left\{\left(\sum_{L=0}^{m} k^{(L)} - i\right)T_s\right\}$$

$$\times G\{iT_s + \beta^{(m)} - T_b/2\} \tag{11}$$

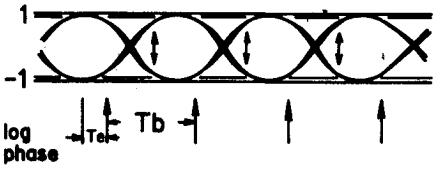
This $\{S[(m-\frac{1}{2})T_b]\}$ has a particular characteristic of taking a zero level, when data change from -1 to $+1$ or from $+1$ to -1, as shown in Fig. 5b. When the sampling timing is correct, the mean value for $\{S[(m-\frac{1}{2})T_b]\}$ has an approximately zero level. For obtaining $\{S(mT_b)\}$ in a good eye-opening condition, the timing adaptation must be carried out so that the $\{S[(m-\frac{1}{2})T_b]\}$ sequence may maintain a zero mean value. An inaccurate timing lag or lead tracing can be detected by using a combination of the sign for $\{S[(m-\frac{1}{2})T_b]\}$ and signal transition, as shown in Figs. 5c



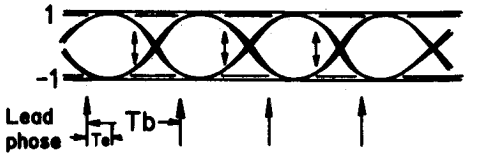
a) Optimum sampling $\{S(mT_b)\}$.



b) $T_b/2$ offset sampling $\{S(m-\frac{1}{2})T_b\}$.



c) Sampling in the lag phase.



d) Sampling in the lead phase.

Fig. 5 Sampling in various phases.

and 5d. For example, during the sampling lag phase when the data change form +1 to −1, $\{S[(m-\frac{1}{2})T_b]\}$ takes on a minus value. When the data change from −1 to +1, $\{S[m-\frac{1}{2}]T_b\}$ takes on a plus value. Therefore, the timing error can be detected by a procedure shown in Fig. 6. With this scheme, the mean value for the detected clock timing error becomes negative under the lead phase condition. It becomes positive under the lag phase condition.

T_c and r are defined as a timing control step size and the sign of a clock timing error in Fig. 6, respectively. The clock timing is controlled by changing the time argument for $G(t)$ in the rate conversion filter, according to the $T_c r$ value. In actuality, Eq. (4), in which the sequence $\{S(mT_b)\}$ is defined values in the eye-opening point, is modified by taking into account sampling phase offsets and frequency differences, as

$$mT_b+\alpha+\sum_{J=0}^{m-1}\gamma^{(J)}=jT_s+\beta^{(m)} \tag{12}$$

where α is the clock phase offset and γ the phase increment caused by the clock frequency difference between the transmitter and receiver.

By introducing $r^{(m)}$, indicating a sign of timing error detected from the mth output data $S(mT_b)$, Eq. (4) can be expressed as

$$mT_b+\alpha+\sum_{J=0}^{m-1}\gamma^{(J)}+T_c\sum_{J=0}^{m-1}r^{(J)}=\sum_{L=0}^{m}k^{(L)}T_s+\beta^{(m)}+T_c\sum_{J=0}^{m-1}r^{(J)} \tag{13}$$

Since a cumulative value of the controlled clock phase

$$T_c\sum_{J=0}^{m-1}r^{(J)}$$

is determined so as to satisfy the equation,

$$-T_c\sum_{J=0}^{m-1}r^{(J)}\approx\alpha+\sum_{J=0}^{m-1}\gamma^{(J)} \tag{14}$$

$$mT_b=\sum_{L=0}^{m}k^{(L)}T_s+\beta^{(m)}+T_c\sum_{J=0}^{m-1}r^{(J)} \tag{15}$$

then

$$S(mT_b)=\sum_{i=-N/2}^{N/2}A\left\{\left(\sum_{L=0}^{m}k^{(L)}-i\right)T_s\right\}\times G\left(iT_s+\beta^{(m)}+T_c\sum_{J=0}^{m-1}r^{(J)}\right) \tag{16}$$

If the argument t of the impulse reesponse $G(t)$ becomes large, due to the introduction of

$$\sum_{J=0}^{m-1}T_c r^{(J)}$$

Eq. (16) cannot produce correct values, because $G(t)$ is being truncated by the summation within the limited range from $-N/2$ to $N/2$. A remedy to prevent this is as follows.

The right side of Eq. (15) can always be modified as

$$\sum_{L=0}^{m}k^{(L)}T_s+\beta^{(m)}+T_c\sum_{J=0}^{m-1}r^{(J)}=\sum_{L=0}^{m}k'^{(L)}T_s+\beta'^{(m)} \tag{17}$$

by using a pair of revised parameters k' and β', instead of k and β. Parameters k' and β' are determined by the following equations:

$$k'^{(m)}=\text{int}\left[\frac{T_b+T_c r^{(m-1)}+\beta'^{(m-1)}}{T_s}\right]$$

$$\beta'^{(m)}=T_b+\beta'^{(m-1)}-k'^{(m)}T_s+T_c r^{(m-1)} \tag{18}$$

$$S(mT_b)=\sum_{i=-N/2}^{N/2}A\left\{\left(\sum_{L=0}^{m}k'^{(L)}-i\right)T_s\right\}\times G(iT_s+\beta'^{(m)}) \tag{19}$$

With these equations and the flow chart shown in Fig. 6, the rate conversion filter takes the form of an adaptive rate conversion filter and its conversion ratio is controlled for generating the optimum eye-opening value. An above-mentioned adaptation is performed in the ARC filter shown in Fig. 7. It can be seen that this structure is very simple compared with that shown in Figs. 3a or 3b.

Adaptive Rate Conversion Filter Performance

Simulated timing control performances for the proposed ARC filter are described in this section. Figure 8 shows that the stable clock timing tracing can be obtained, even under 10 dB carrier-to-noise ratio (C/N) conditions, without a clock phase slipping. Figure 9 shows timing error convergence during the clock acquisition process from a phase error. Figure 10 shows the eye scatter diagram in the QPSK acquisition process at 0 dB C/N. The simulation is begun from ½ T_B phase offset separate from the eye-opening point. Widely scattered interpolation signals are gradually controlled for obtaining eye-opening values and the correct clock phase timing is finally maintained. Highlighted parts show the four signal points of QPSK after acqusition. In this figure, the noise introduced in the simulation is removed for obtaining a clear scatter diagram.

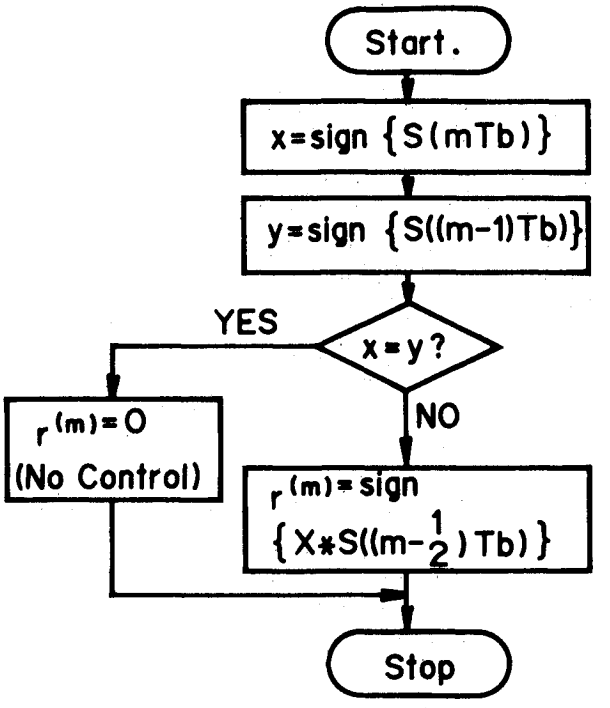


Fig. 6 Timing error detection flow chart.

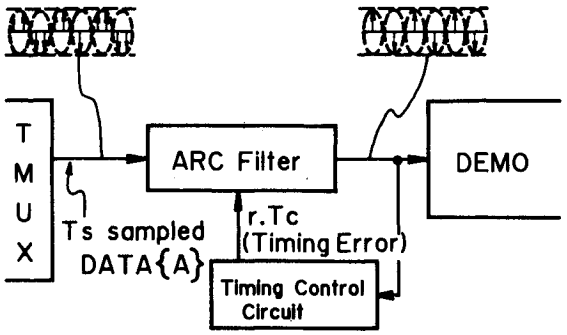


Fig. 7 ARC filter configuration.

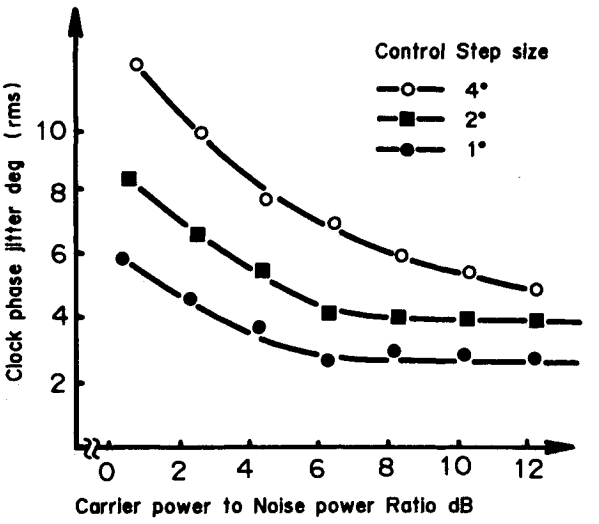


Fig. 8 Simulated clock phase jitter performance.

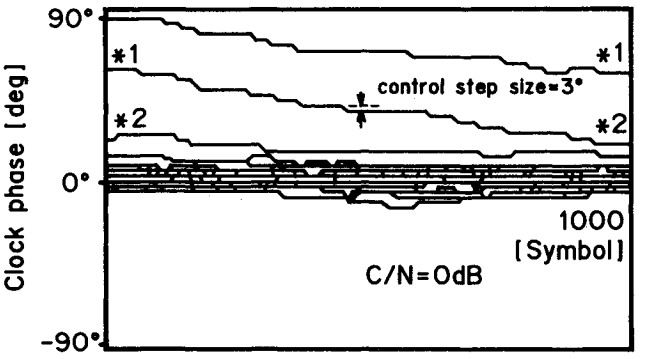


Fig. 9 Simulated clock phase jitter performance.

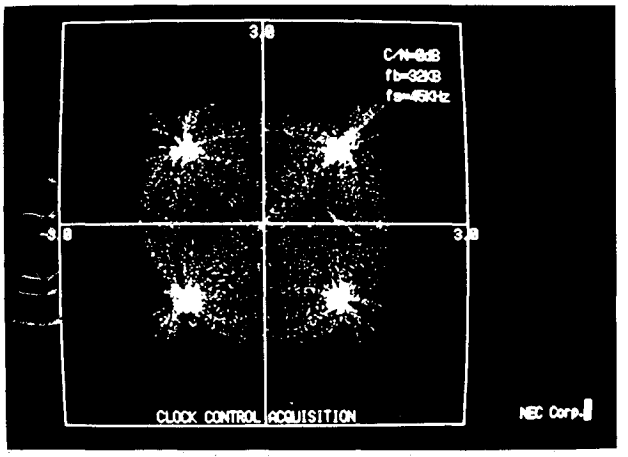


Fig. 10 ARC filter acquisition process.

Carrier Recovery

Since each carrier frequency is an independent element and has carrier frequency offset Δf, the signal is converted to the Δf frequency shifted baseband signal by the TMUX. Therefore, the carrier recovery function, by employing a digital phase-locked loop (PLL),[6] is required for each channel demodulator. There can be two loop configuration methods, as shown in Fig. 11. Although the Fig. 11a configuration is easy to implement, the signal suffers degradation from the ARC filter band limitation, by which the band edge of the demodulated signal is cut down, as shown in spectrum 3. If the carrier offset is eliminated before the ARC filter by use of the method 2 (Fig. 11b), no degradations occur to an output signal, as can be seen in spectrum 3′. Consequently, the latter is favorable for use as a low-degradation receiver, although it has two different operational clock values. This structure is adopted for the proposed implementation model. Figure 12 shows a simulated result on the scatter diagram in an acquisition process, under 2 dB C/N and $f_s/1024$ carrier offset conditions. In Fig. 12, widely scattered signal points and the brighter part on the circle indicate the conditions before and after the clock and carrier are recovered, respectively. In the simulation, as the clock timing acquisition is finished more rapidly than the carrier phase acquisition, only the carrier phase relation remains in the pattern of a circle.

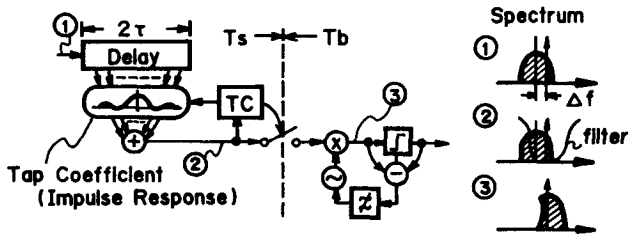
As before, noise in the simulation is removed for display purposes.

Channel Demodulator Hardware

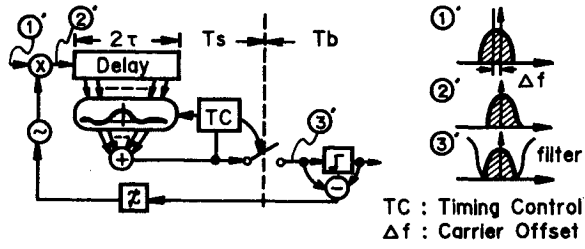
A channel demodulator, based on the proposed ARC filter, has been developed to comply with the INTELSAT SCPC system specificiation. The modulation method is QPSK and f_s and f_b are set to be 45 and 32 kHz, respectively.

Figure 13 shows the channel demodulator configuration. It consists of the interpolation, clock recovery, carrier recovery, and AGC circuits. The interpolation and clock timing control follow the proposed ARC filtering action. In this figure, the ARC filter, located in the center, consists of a first-in/first-out memory (FIFO), transversal filter, and timing control circuit. In order to maintain the sampling points in the best eye-opening condition, the rough control is carried out by controlling the number of sampled data taken into the transversal filter. Fine control is performed by selecting the tap weight set corresponding to k' and β', respectively.

Table 1 summarizes the number of components and power consumption for the developed QPSK channel demodulator. Figures 14 and 15 show the baud rate sampled eye pattern during the clock acquisition process, under the noise-free condition by use of the developed circuit board. These output eye patterns are controlled to 4 deg step size. Figure 15 shows expanded time division eye pattern. Figures 16 and 17 show the steady-state eye scatter diagram from the developed channel demodulator output obtained from 60 Hz carrier offset, with 5 dB C/N and noise free, respectively.



a) Method 1.



b) Method 2.

Fig. 11 Carrier recovery configuration methods.

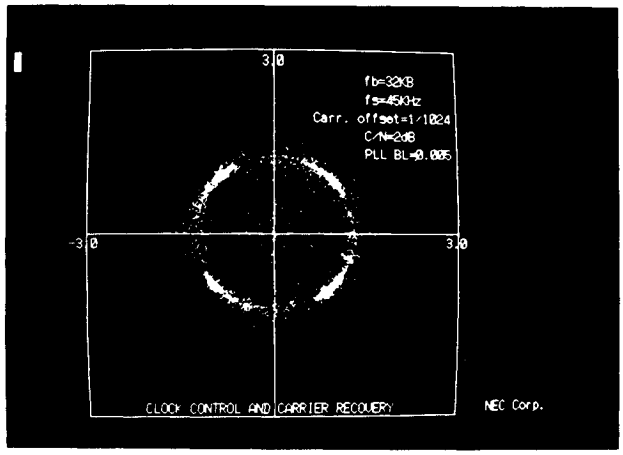


Fig. 12 Carrier recovery acquisition process.

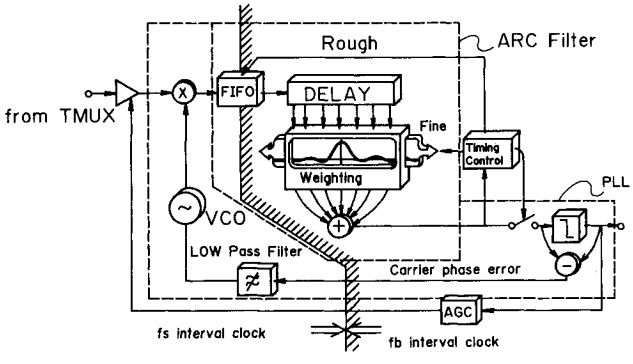


Fig. 13 Channel demodulator configuration.

Table 1 Number of parts in digital channel demodulator (4.0 W total power)

Interpolation and clock recovery	Carrier recovery and AGC
DSP×1 FIFO×2 TTL×7	DSP×2 TTL×24

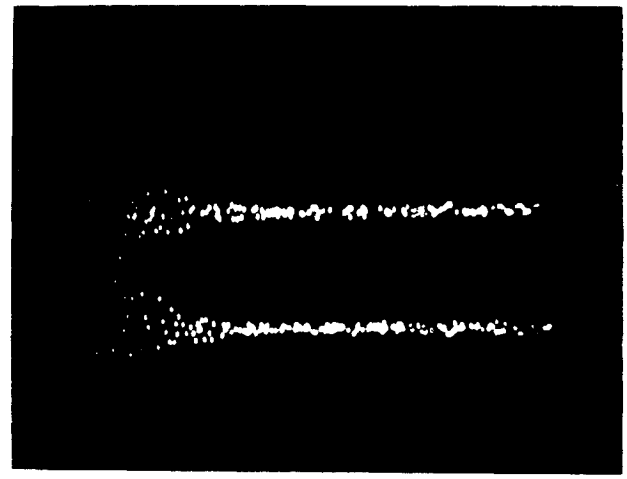


Fig. 14 Clock acquisition.

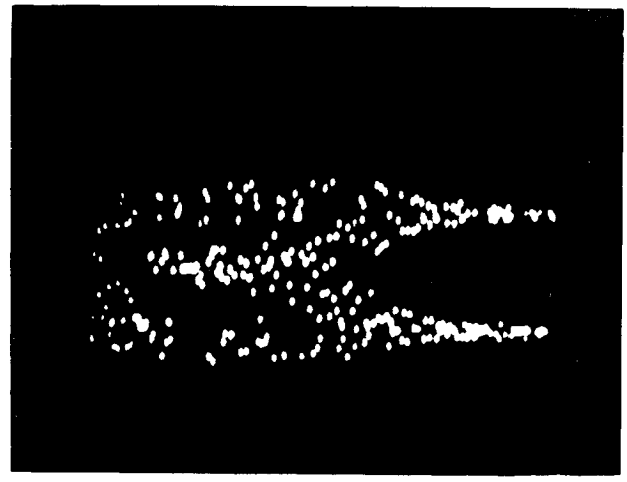


Fig. 15 Clock acquisition (expanded time division).

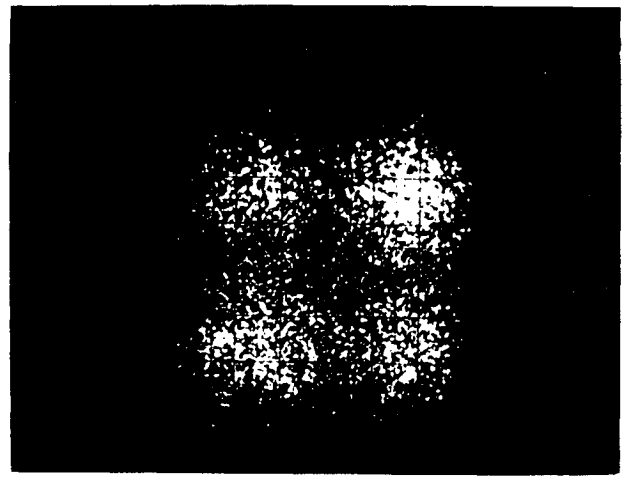


Fig. 16 5 dB C/N eye diagram.

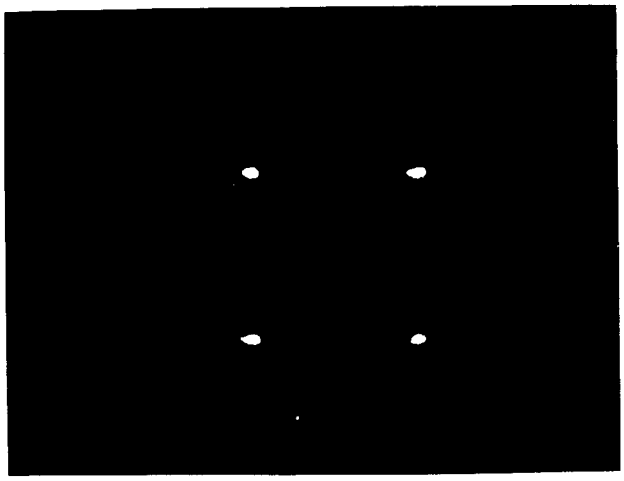


Fig. 17 Noise free eye diagram.

Conclusion

A digital group demodulator has been implemented by employing a transmultiplexer (TMUX) that simultaneously translates multiple SCPC carrier signals into the original baseband form. Since the operation rate for the TMUX is determined by the channel spacing and not by the baud rate, an adaptive interpolation function is required for each channel following the TMUX operation, so that the baseband signals can be obtained at the correct decision timing. For this purpose, an adaptive rate conversion (ARC) filter has been introduced. Using the ARC filters, excellent demodulation performance is always obtained for any relation between the channel spacing and the baud rate in an SCPC system. The ARC filter operation rate for each channel is equal to the symbol rate for that channel, so it is possible to realized one filter by a single-chip digital signal processor. An implemented ARC filter has worked well in a 16 channel digital group demodulator for a 64 kb/s SCPC system. In the near future, it will become possible to implement a single-chip ARC filter that provides an interpolation operation for as many as 100 SCPC channels, it a ROM table look-up method is used instead of digital multiplication for the filter tap weight calculation.

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